

a layer of metal that will be etched to form conductive interconnects from one portion of the semiconductor device 100 that will form pads that will be connected to external structures during the gold wire bonding process. The layer 104 is typically formed from aluminum. A layer 106 of TiN is formed on the surface of the layer 104. The layer 106 of TiN serves as both a barrier layer and as an anti-reflective coating. A layer 108 of photoresist is formed on the surface of the layer 106 of TiN.

Figure 1B shows the partially completed semiconductor device 100 as shown in **Figure 1A** with the layer of photoresist 108 patterned and developed forming holes 110 and 112 in the layer 108 of photoresist that expose portions of the layer 106 of TiN.

Figure 1C shows the partially completed semiconductor device 100 as shown in **Figure 1B** after an etch process to etch the exposed portions of the layer 106 of TiN and exposing portions of the metal layer 104.

Figure 1D shows the partially completed semiconductor device 100 as shown in **Figure 1C** after an etch process to etch the exposed portions of the metal layer 104 down to the surface of the layer 102 of interlayer dielectric.

Figure 1E shows the partially completed semiconductor device 100 as shown in **Figure 1D** with the layer of photoresist 108 removed.

Figure 1F shows the partially completed semiconductor device 100 as shown in **Figure 1E** with a blanket layer 114 of interlayer dielectric formed on the surface of the semiconductor device 100 and filling the holes 110 and 112.

Figure 1G shows the partially completed semiconductor device 100 as shown in **Figure 1F** after a layer 116 of photoresist is formed on the surface of the layer 114 of interlayer dielectric. The layer 116 of photoresist is patterned and developed to form holes 118, 120, and 122 that expose portions of the layer 114 of interlayer dielectric.

Figure 1H shows the partially completed semiconductor device 100 as shown in **Figure 1G** after an etch process to etch exposed portions of the layer 114 of interlayer dielectric exposing portions of the layer 106 of TiN.

Figure 1I shows the partially completed semiconductor device 100 as shown in **Figure 1H** after an etch process to etch the exposed portions of the layer 106 of TiN.

The step of completely etching the layer 106 of TiN during the pad etch process causes a slow down in the throughput of the semiconductor device during the manufacturing process.

Therefore, what is needed is a manufacturing process that does not require the step of etching the TiN layer during pad etch.

SUMMARY OF THE INVENTION

According to the present invention, the foregoing and other objects and advantages are obtained by a method of manufacturing semiconductor devices wherein a layer of TiN overlying metal structures in the final metal layer is removed after final metal
5 etch. In accordance with one aspect of the invention, the method involves forming a final layer of metal on a layer of interlayer dielectric, forming a layer of TiN on the final layer of metal, forming a layer of photoresist on the layer of TiN, patterning and developing the layer of photoresist exposing portions of the final metal layer, and etching the exposed
10 portions of the final metal layer forming metal structures. The layer of photoresist and layer of TiN are removed.

In another aspect of the invention, a blanket layer of interlayer dielectric is formed on the surface of the semiconductor device after the layer of photoresist and layer of TiN are removed. A second layer of photoresist is patterned and developed exposing portions
15 of the interlayer dielectric overlying the metal structures. The exposed portions of the interlayer dielectric are etched down to the surface of the metal structures.

In still another aspect of the invention, the layer of photoresist and the layer TiN are removed by a process utilizing fluorine containing gas chemistry at an elevated temperature.

20 The described method of manufacturing semiconductor devices thus provides a method of removing the layer of TiN formed on the final metal layer structures resulting in improved throughput during pad etch.

The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become
25 readily apparent to those skilled in the art from the following description, there is shown and described an embodiment of this invention simply by way of illustration of the best mode to carry out the invention. As will be realized, the invention is capable of other embodiments and its several details are capable of modifications in various obvious aspects, all without departing from the scope of the invention. Accordingly, the drawings
30 and detailed description will be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and

further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figures 1A – 1J show a prior art method of manufacturing a semiconductor device in which a layer of TiN formed on a metal structure is etched during the pad etch process, wherein;

Figure 1A shows a partially completed semiconductor device showing the final metal layer with a layer of TiN formed on the metal layer and a layer of photoresist formed on the layer of TiN;

Figure 1B shows the partially completed semiconductor device as shown in **Figure 1A** with the layer of photoresist patterned and developed forming holes in the photoresist exposing portions of the layer of TiN;

Figure 1C shows the partially completed semiconductor device as shown in **Figure 1B** after an etch process etches the exposed portions of the layer of TiN exposing portions of the metal layer;

Figure 1D shows the partially completed semiconductor device as shown in **Figure 1C** after an etch process etches the exposed portions of the metal layer exposing portions of a layer of interlayer dielectric underlying the metal layer;

Figure 1E shows the partially completed semiconductor device as shown in **Figure 1D** with the layer of photoresist removed;

Figure 1F shows the partially completed semiconductor device as shown in **Figure 1E** with a blanket layer of interlayer dielectric formed on the surface of the semiconductor device;

Figure 1G shows the partially completed semiconductor device as shown in **Figure 1F** after a layer of photoresist has been formed on the surface of the layer of interlayer dielectric and after the layer of photoresist has been patterned and developed exposing selected portions of the layer of interlayer dielectric;

Figure 1H shows the partially completed semiconductor device as shown in **Figure 1G** after an etch process to etch the exposed portions of the layer of interlayer dielectric down to the layer of TiN;

Figure 1I shows the partially completed semiconductor device as shown in **Figure 1H** after an etch process to etch the exposed layer of TiN;

Figures 2A – 2G show a method of manufacturing a semiconductor device in accordance with the present invention; wherein;

Figure 2A shows the partially completed semiconductor device as shown in **Figure 1D** after the layer of photoresist has been removed;

Figure 2B shows the partially completed semiconductor device as shown in **Figure 2A** after the layer of TiN has been removed from the surfaces of metal structures
5 formed in previous processing steps;

Figure 2C shows the partially completed semiconductor device as shown in **Figure 2B** with a blanket layer of interlayer dielectric formed on the surface of the semiconductor device;

Figure 2D shows the partially completed semiconductor device as shown in
10 **Figure 2C** after a layer of photoresist has been formed on the surface of the layer of interlayer dielectric and after the layer of photoresist has been patterned and developed exposing selected portions of the layer of interlayer dielectric;

Figure 2E shows the partially completed semiconductor device as shown in **Figure 2D** after an etch process to etch the exposing portions of the layer of interlayer
15 dielectric; and

Figure 2F shows the partially completed semiconductor device as shown in **Figure 2E** after the layer of photoresist has been removed.

DETAILED DESCRIPTION

20 Reference is now made in detail to specific embodiments of the present invention which illustrate the best mode presently contemplated by the inventors for practicing the invention.

Figures 2A –2G show a method manufacturing a semiconductor device in accordance with the present invention.

25 **Figure 2A** shows the partially completed semiconductor device **100** as shown in **Figure 1D** with the layer **108** of photoresist removed.

Figure 2B shows the partially completed semiconductor device **100** as shown in **Figure 2A** with the layer **106** of TiN removed. The layer **108** of photoresist and the layer **106** of TiN are stripped during the same process step. One such method is to use a
30 fluorine containing gas chemistry at elevated temperatures. For example, it has been shown that TiN and the resist can be removed effectively using a CF_4/O_2 gas chemistry at elevated temperatures. Typical applied power is in a range of 500 to 1000W at a pressure in a range of 500 to 2000mTorr. Typical gas flow rates are in the range of 100 to 500 sccm. The TiN removal rate is strongly dependent on the wafer temperature and CF_4 gas

flow, with higher removal rates at higher temperature and higher flow rates. TiN removal rates in excess of 2000Å/minute were achieved at 120°C wafer temperature, with substantially higher removal rates as temperatures were increased up to 240°C. This has been demonstrated in both an inductively-coupled resist stripper and a downstream
5 microwave resist stripper.

Figure 2C shows the partially completed semiconductor device **100** as shown in **Figure 2B** with a blanket layer **114** of interlayer dielectric formed on the surface of the semiconductor device **100** and filling the holes **110** and **112**.

Figure 2D shows the partially completed semiconductor device **100** as shown in
10 **Figure 2C** after a layer **116** of photoresist is formed on the surface of the layer **114** of interlayer dielectric. The layer **116** of photoresist is patterned and developed to form holes **118**, **120**, and **122** that expose portions of the layer **114** of interlayer dielectric.

Figure 2E shows the partially completed semiconductor device **100** as shown in **Figure 2C** after an etch process to etch exposed portions of the layer **114** exposing
15 portions of the layer **104**.

Figure 2F shows the partially completed semiconductor device **100** as shown in **Figure 2E** with the layer **116** of photoresist removed.

In summary, the results and advantages of the method of the present invention can now be fully realized. The method of removing the layer of TiN after final metal etch thus
20 provides increased throughput during pad etch.

The foregoing description of the embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to
25 provide the best illustration of the principles of the invention and its practical application to thereby enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to
30 which they are fairly, legally, and equitably entitled.